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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,705	11/21/2003	Naoki Yamamoto	HITA.0462	8848

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EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,705	YAMAMOTO, NAOKI	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9,10,13,14 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11,12,15-18 and 20* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1103*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-8, 11, 12, 15-18 and 20 in the reply filed on October 8, 2004 is acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The references cited within the IDS document, received on November 21, 2003 have been considered.

Claim Objections

4. Claim 15 is objected to because of the following informalities:

Line 3 of claim 15 refers to a "metal *carbide* film" on the polycrystalline silicon, but then refers to a "metal *nitride* film" in line 4. For purposes of examining this claim, the examiner will assume the first mention of "metal carbide" to be a "metal nitride" (which would result in a gate stack layered structure of polycrystalline silicon, then metal nitride and then metal, as is shown by applicant's figures 2 and 3). Applicant is advised to amend this claim to avoid an issue with 35 USC 112, second paragraph.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 3, 11, 12, 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,323,519 B1) in view of Tai (6,686,277 B1).

6A. As to **claim 1**, Gardner et al. teach a process for forming an integrated circuit device, as shown in figures 1-9. A semiconductor substrate **12** is provided, as shown in figure 1. Also depicted in figure 1, are a gate insulator (i.e. gate dielectric) layer **16** formed on the substrate **12** and a conducting film (i.e. gate conductor) **18** formed atop the gate dielectric layer **16**. The gate dielectric and gate conductor layers are patterned to form a gate electrode (see also column 6, lines 59-67, continued to column 7, lines 1-30). A nitriding step is performed as shown in figure 3 on the sidewalls of the gate electrode structure, resulting in nitrided oxide layer **24**. This step is performed at a temperature range of 300-700°C (see also column 8, lines 13-35). The main surface of the substrate is then oxidized as shown by figure 9 (see also column 9, lines 52 et seq.).

Gardner et al. do not teach the conducting film to be a metal film or a metal compound film. Rather, Gardner et al. teach the conducting film **18** to be polysilicon (see column 7, lines 20-30).

However, Tai teaches a similar method of forming an integrated circuit device wherein the conducting film of the gate electrode is metal; specifically, Tai teaches it to be tungsten (see figures 1b and 1c, numerals 6 and 6' and also column 2, lines 64-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the process of forming an integrated circuit device of Gardner et al. with a metal layer (e.g. tungsten) as taught by Tai since tungsten can withstand higher processing temperatures than polysilicon without the risk of degradation or damage.

6B. As to **claim 2**, Gardner et al. teach the nitriding step to be performed at a temperature range of 300-700°C (see also column 8, lines 13-35).

6C. As to **claim 3**, Gardner et al. teach the nitriding step to be a nitrogen plasma, and the nitriding step is performed on the sidewalls of the gate electrode structure (see also column 8, lines 13-35).

6D. As to **claim 11**, Tai teaches forming a gate electrode stack structure, as shown in figure 1c, of polycrystalline silicon **4'**, a metal nitride (tungsten nitride) **5'** on the polycrystalline silicon and a metal (tungsten) **6'** on the metal nitride layer.

6E. As to **claim 12**, Tai teaches the metal nitride layer **5'** to be tungsten nitride and the metal layer **6'** to tungsten.

6F. As to **claim 15**, Tai teaches a gate electrode having a layered structure of polycrystalline silicon layer **4'**, a metal nitride layer **5'** and a metal layer **6'**, as shown in figure 1C.

6G. As to **claim 16**, Tai teaches the tungsten metal layer **6'** of the gate electrode stack **8** in figure 1c to be a single layer (i.e. one layer) of tungsten deposited by a sputtering technique (see also column 2, lines 64 et seq.).

6H. As to **claim 18**, Gardner et al. teach a process for forming an integrated circuit device, as shown in figures 1-9. A semiconductor substrate 12 is provided, as shown in figure 1. Also depicted in figure 1, are a gate insulator (i.e. gate dielectric) layer 16 formed on the substrate 12 and a conducting film (i.e. gate conductor) 18 formed atop the gate dielectric layer 16. The gate dielectric and gate conductor layers are patterned to form a gate electrode (see also column 6, lines 59-67, continued to column 7, lines 1-30). A nitriding step is performed as shown in figure 3 on the sidewalls of the gate electrode structure, resulting in nitrided oxide layer 24. This step is performed at a temperature range of 300-700°C (see also column 8, lines 13-35). The main surface of the substrate is then oxidized as shown by figure 9 (see also column 9, lines 52 et seq.).

Gardner et al. do not teach the conducting film to be a metal film or a metal compound film. Rather, Gardner et al. teach the conducting film 18 to be polysilicon (see column 7, lines 20-30). Gardner et al. also do not teach forming a first insulator film on top of the conducting film before patterning of the conducting film, wherein the insulator film remains on top of the conductor film during the nitriding step.

However, Tai teaches a similar method of forming an integrated circuit device wherein the conducting film of the gate electrode is metal; specifically, Tai teaches it to be tungsten (see figures 1b and 1c, numerals 6 and 6' and also column 2, lines 64-65).

Tai also teaches forming an insulator film (silicon nitride) 7 on top of the conducting film (tungsten) 6 as shown in figure 1b. As shown in further figures 1c and 2a, the silicon nitride insulator film remains on top of the tungsten conducting film, after patterning of the layers to form the gate electrode (figure 1c) and after the nitriding step (figure 2a).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the process of forming an integrated circuit device of Gardner et al. with a metal layer as the gate conductor and with an insulator layer as taught by Tai since a metal gate conductor (e.g. tungsten) can withstand higher processing temperatures than polysilicon without the risk of degradation or damage, and an insulator layer atop the gate conductor layer provides additional protection for the gate conductor.

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7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,323,519 B1) and Tai (6,686,277 B1) as applied to claim 1 above, and further in view of Swanson et al. (6,262,445 B1).

7A. As to **claim 4**, Gardner et al. and Tai teach all of the limitations of claim 4, as noted above for claim 1, except for carbonizing a sidewall with a carbon-containing gas, under conditions of heat-treatment or plasma treatment. However, Swanson et al. teach carbonizing (i.e. forming a carbide layer) on a gate electrode, as depicted by figures 1 and 2. The gate structure **30**, with oxide layer **40**, is carbonized by depositing a silicon carbide layer and etching to form sidewalls **60**. The silicon carbide is deposited by plasma enhanced chemical vapor deposition (column 2, lines 50-53) using a carbon

containing gas, such as methane (see table, column 2, lines 55-63). It would have been obvious to a person of ordinary skill in the art to modify the method of Gardner et al. and Tai with a carbonizing treatment as taught by Swanson et al. so as to form silicon carbide sidewall structures, since good quality silicon carbide can be deposited at temperatures lower than 600°C and silicon carbide can be etched selective to oxide (see also column 1, lines 54-62).

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8. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,323,519 B1) and Tai (6,686,277 B1) as applied to claim 1 above, and further in view of Segawa et al. (6,518,636 B2).

8A. As to **claims 5-7**, Gardner et al. and Tai teach all of the limitations of claims 5, 6 and 7, as noted above for claim 1, except for oxidizing a main surface of the semiconductor substrate by plasma using an oxygen-containing gas, oxidizing at a temperature of 600°C or lower, and more specifically oxidizing at a temperature of 200°C to 500°C. However, Segawa et al. teach oxidizing a main surface of the substrate using a plasma and an oxygen-containing gas. Segawa et al. also teach performing the oxidizing step at a temperature of 150°C to 300°C (see column 7, lines 59-67, continued to column 8, lines 1-8). It would have been obvious to a person of ordinary skill in the art to modify the method of Gardner et al. and Tai with an oxidizing step as taught by Segawa et al. so as to provide a protective layer for the substrate for subsequent processing steps.

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9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,323,519 B1) and Tai (6,686,277 B1) as applied to claim 1 above, and further in view of Wieczorek et al. (6,306,698 B1).

9A. As to **claim 17**, Gardner et al. and Tai teach all of the limitations of claim 17, as noted above for claim 1, except for a gate stack structure of a polycrystalline silicon film and a metal silicide film on the polycrystalline film. However, Wieczorek et al. teach a gate electrode stack comprising a polycrystalline silicon film layer 104 and a metal silicide film layer 111A on the polycrystalline silicon layer, as shown in figure 2D. It would have been obvious to a person of ordinary skill in the art to modify the method of Gardner et al. and Tai with a gate stack structure including a metal silicide as taught by Wieczorek et al. since metal silicide layers atop polycrystalline silicon layers in gate electrode stacks aide in lowering the resistance of the gate electrode structure (see also column 2, lines 7-17).

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10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (6,323,519 B1) and Tai (6,686,277 B1) as applied to claim 1 above, and further in view of Samavedam et al. (6,514,808 B1).

10A. As to **claim 20**, Gardner et al. and Tai teach all of the limitations of claim 20, as noted above for claim 1, except for providing for removing a portion of the gate insulator film below the conducting film to be removed when patterning the conducting film. However, Samavedam et al. teach removing a portion of the gate insulator film **24** that is beneath the conducting portion **16** of the gate structure during gate structure

formation, as shown in figure 2. It would have been obvious to a person of ordinary skill in the art to modify the method of Gardner et al. and Tai with a gate insulator layer removal (i.e. undercutting) as taught by Samavedam et al. so as to reduce the Miller capacitance of the transistor structure (see also column 2, lines 9-21).

Allowable Subject Matter

11. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a fabrication process including a step of restoring damages in the gate insulator film near the gate electrode through oxidizing the main surface of the gate insulator film. Kohyama et al. (6,608,356 B1) teach repairing damage using oxidation, but do not specifically teach restoring damages in a gate insulator film near the end of gate electrode.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571)272-2034. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT GEYER
PATENT EXAMINER

SBG
December 21, 2004

12/21/04